REMARKS

This amendment is in response to the non-final Office Action mailed October 18, 2007. Claims 1 and 3-23 are currently pending. Claims 1, 2, 7-9, and 13-16 stand rejected. Claims 1, 3, 5, 9, and 15 have been changed, claim 2 has been cancelled, and claims 17-23 have been added by this amendment. No new matter has been added. Reconsideration of the present application in view of the amendments and remarks that follow is respectfully submitted.

The amendments to the claims are fully supported by the specification. Claims 1 and 24 recite first rotate up and rotate down signals causing rotation of a phase of a signal up or down to compensate for the frequency offsets, as described at page 2, lines 9-14, page 4, lines 3-7 and 12-13, and page 5, lines 17-23. Claims 1 and 24 also recite that second rotate-up and rotate-down signals improve a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets, as described at page 5, lines 8-12 and 15-21, and page 6, lines 3-8. The other amendments and the new claims recite subject matter of existing claims.

§102 REJECTIONS

The Examiner rejected claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,075,948 ("Makarov"). Applicant respectfully traverses, and has amended the claims for clarification.

Makarov discloses a frequency offset estimator including a counter-clockwise transition detector 102 and a clockwise transition detector 104 that output signals D to a counter 108 including a clockwise accumulator and a counter-clockwise accumulator. The accumulators count the signals D over a given time period and output counts N to a processing component including an adder 116 that differences the counts to determine sign and magnitude of the frequency offset.

Makarov does not disclose or suggest the invention of claim 1. Claim 1 recites a controller that generates first rotate up and rotate down signals for phase adjusts to adapt to frequency offsets, the first signals causing rotation of the phase up or down to compensate for the frequency offsets. Claim 1 also recites an adjust circuit that detects trends in the first rotate-up and rotate-down signals, and generates second rotate-up and rotate-down signals that improve the rate of compensation for the frequency offsets, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets. Makarov does not disclose or suggest an adjust circuit that detects trends in previously-generated rotate up and rotate down signals, nor discloses or suggests a circuit that generates second rotate up and rotate down signals that improve the rate of compensation for frequency offsets relative to using only the first signals.

Makarov discloses a circuit 100 of Fig. 5 that counts detected occurrences of transition events in a received signal (col. 6, lines 35-36) and adds up these detected occurrences in counter 108 and differences clockwise and counterclockwise counts in adder 116 to determine sign and magnitude. Nowhere does Makarov disclose or suggest detecting trends in signals used for rotating a phase of a clock signal. Makarov only discloses counting transitions to detect the magnitude and direction of an offset. Furthermore, Makarov does not disclose or suggest generating second rotate up and rotate down signals for improving compensation of frequency offsets relative to compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets. Makarov discloses only detecting the sign and magnitude of a frequency offset, not generating second rotate signals for improving compensation relative to generated first rotate signals.

The Examiner stated that Makarov's detectors 102 and 104 read on claim 1's controller for generating first signals, and that Makarov's counter 108 and processing circuit 112 read on claim 1's adjust circuit. However, this is not possible, since Makarov's detectors 102 and 104 generate signals D that indicate a detected occurrence of a transition event in the signal in clockwise or counterclockwise directions, and these signals D are not rotate up and rotate down signals for rotating a phase up or down. The D signals simply indicate a transition in a signal. Furthermore, Makarov's counters 108

do not detect trends in the first rotate signals, since these counters 108 simply count transitions, not detect trends in signals used to rotate a phase of a clock. In addition, the adder 116 does not generate the second rotate signals recited in claim 1, since the adder simply differences the count signals from the counters 108 and does not generate rotate-up and rotate-down signals.

The Examiner stated (with regard to claim 2) that Makarov discloses second rotate-up and rotate-down signals as the N count signals provided from the counters 108(1) and 108(2). However, these N count signals cannot be the second rotate signals recited in claim 1 because the N count signals do not improve the rate of compensation relative to compensation provided by using only the first rotate-up and rotate-down signals. The N count signals simply provide a count of transitions, and do not improve compensation relative to first compensation rotate signals.

Furthermore, Makarov does not disclose or suggest using combinatorial logic to adapt the first signals based on accumulated data accumulated by an accumulator. The Examiner stated that Makarov's adder 116 of Fig. 5 reads on claim 1's combinatorial logic, but if so, Makarov does not disclose or suggest any accumulator different than the combinatorial logic as recited in claim 1. Counters 108 are not an adder as recited in claim 1.

Applicant therefore believes that claim 1 is patentable over Makarov. Accordingly, Applicant respectfully requests that the rejection of claims 1 and 2 under 35 U.S.C. 102(e) be withdrawn.

The Examiner rejected claims 7, 8, 13, and 14 under 35 U.S.C. 102(b) as being anticipated by Usui (U.S. Patent No. 6,269,128) ("Usui '128"). Applicant respectfully traverses.

Usui '128 discloses a clock recovery circuit including a lead/lag detector 210 that determines whether a phase signal leads or lags behind a corresponding ideal phase. An up/down counter 211 receives an up/down signal from lead/lag detector 210 and increments or decrements a counter by a magnitude indicated by a corrective width

signal. The counter 211 and self running counter 212 are added by a full adder 213 to output a symbol clock signal.

In contrast, claim 7 recites an up/down counter for counting signals from a phase rotator control for phase adjustments by a clock-data-recovery loop of a serial receiver, and an adder coupled to the up/down counter that outputs accumulated data indicative of a trend in the phase adjustments. Usui '128 does not disclose or suggest an adder that outputs accumulated data indicative of a trend in phase adjustments. Usui '128's adder adds the count outputs of the up/down counter 211 and self-running counter 212 which are used to generate an adjusted clock signal that has been corrected for interference in the phase. The BWD signal from the clock corrective section is used to adjust the up/down counts of the up/down counter based on interference in the signal (col. 6, lines 2-4). Usui '128's circuit looks at lead or lag in incoming signals to adjust a clock signal to compensate for interference. This is different from Applicant's claim 7, in which accumulated data is output indicative of a trend in phase adjustments. Applicant's invention indicates trends in the adjustments to the phase, which is not the same as performing the adjustments themselves in the phase or signal. Usui '128 describes performing an actual adjustment to the phase or signal, but does not disclose or suggest indicating a trend in multiple phase adjustments.

The Examiner stated that the counts of the up/down counter 211 and the self running up counter 212 are added by the full adder 213 to produce the symbol clock, where the up/down counter is accumulating the up/down signal output by the lead/lag detector for a period of time, and the output of the adder is indicative of the trend in the phase adjustment over that period of time. However, the up/down counter 211 is not an adder that accumulates data. Furthermore, the output of the adder 213 is a clock that is indicative of and compensates for leads and lags in an ideal phase (col. 4, lines 58-60). Adder 213 provides a clock that has been adjusted based on the current lead or lag by adjusting (with counter 211) the count provided by the self running up counter 212. This output of the adder 213 thus does not indicate a trend in multiple phase adjustments--it provides only a clock signal that indicates and has been adjusted for current lead or lag.

Applicant therefore believes that claim 7 is patentable over Usui '128. Claim 8 is dependent on claim 7 and is patentable over Usui '128 for at least the same reasons as claim 7, and for additional reasons.

Claim 13 recites a method including monitoring trends of phase adjusts of signals from a phase rotator control of a clock-data-recovery circuit to a reference clock of a serial receiver, and adapting the phase adjusts to create future adjusts based on previous adjusts. Similarly as explained above for claim 7, Usui '128 does not disclose or suggest monitoring trends of phase adjusts of signals from a phase rotator control. Usui '128 discloses outputting a symbol clock that has been corrected for current lead or lag in a signal caused by phase interference, and nowhere discloses or suggests monitoring trends of multiple phase adjusts. Usui '128 adjusts the signals with the circuit of Fig. 2, but does not monitor trends in those adjusts. Usui's up/down counter 211 increments or decrements a counter directly based on whether the signal leads or lags an ideal clock, i.e. directly adjusts the clock signal, but does not monitor trends in multiple such adjustments over time; Usui adjusts the clock according to the currently-detected lag or lead in the signal. Nor does Usui '128 adapt the phase adjusts to create future adjusts based on previous adjusts.

Applicant therefore believes that claim 13 is patentable over Usui '128. Claim 14 is dependent on claim 13 and is patentable over Usui '128 for at least the same reasons as claim 13, and for additional reasons similar to those explained above.

Applicant therefore respectfully requests that the rejection of claims 7, 8, 13 and 14 under 35 U.S.C. 102(b) be withdrawn.

The Examiner rejected claims 9, 15, and 16 under 35 U.S.C. 102(e) as being anticipated by Usui (U.S. Patent No. 6,615,060) ("Usui '060"). Applicant respectfully traverses. Applicant has amended claim 9 to be dependent on claims 7 and 8 and has amended claim 15 to be dependent on claims 13 and 14.

Usui '060 discloses a clock reproducing unit in Fig. 3 which provides a phase data signal to a detecting unit that determines the phase difference between the phase data

signal and the data clock signal, and provides a phase difference signal to an up/down counter that adds or subtracts at the timing of the data clock signal. An adder adds the count from the up/down counter and a counter 143 to provide control signals including the data clock signal.

Similarly to Usui '128 as explained above, Usui '060 does not disclose or suggest an adder that outputs accumulated data indicative of a trend in phase adjustments as recited in claims 7 and 9. Usui '060's adder 144 adds the count outputs of the up/down counter 142 and counter 143 which are used to generate an adjusted clock signal that has been corrected based on a phase difference of phase data signals (col. 6, lines 1-5). Usui '060's circuit looks at phase differences in signals to adjust a clock signal to compensate. This is different from Applicant's claims 7 and 9, in which accumulated data is output indicative of a trend in the adjustments to the phase, which is not the same as performing the adjustments or corrections to the phase or signal. Usui '060 describes performing an actual adjustment or correction to the phase or signal, but does not disclose or suggest indicating a trend in multiple phase adjustments.

The Examiner stated that the up/down counter 142 accumulates up and down signal output and the output of the counter is indicative of a trend in the phase adjustments. However, the up/down counter 142 is not an adder that accumulates data. Furthermore, the output of the up/down counter 142 is a count, and the output of the adder 144 is a clock, either being indicative of a phase difference between signals. These outputs of the counter 142 or adder 144 thus are not indicative of a trend in multiple phase adjustments--they provides only signals that indicate and compensate for current phase difference.

Applicant therefore believes that claim 7 is patentable over Usui '060. Claim 9 is dependent on claim 7 and is patentable over Usui '060 for at least the same reasons as claim 7, and for additional reasons.

Claim 15 is dependent on claim 13, which recites a method including monitoring trends of phase adjusts of signals from a phase rotator control of a clock-data-recovery circuit to a reference clock of a serial receiver, and adapting the phase adjusts to create future adjusts based on previous adjusts. Similarly as explained above for claim 7, Usui

'060 does not disclose or suggest monitoring trends of phase adjusts of signals from a phase rotator control. Usui '060 discloses looking at phase differences in signals to adjust a clock signal to compensate, and nowhere discloses or suggests monitoring trends of multiple phase adjusts. Nor does Usui '060 adapt the phase adjusts to create future adjusts based on previous adjusts.

Applicant therefore believes that claim 13 is patentable over Usui '060. Claims 15 and 16 are dependent on claim 13 and is patentable over Usui '060 for at least the same reasons as claim 13, and for additional reasons similar to those explained above.

Applicant therefore respectfully requests that the rejection of claims 9, 15, and 16 under 35 U.S.C. 102(e) be withdrawn.

NEW CLAIMS

Applicant has added claims 16-23. Claims 16-18 are dependent from claim 13 and recite generating a new rotate up signal based on an overflow in the adder, generating a new rotate down signal based on an underflow in the adder, and an adder accumulating a chosen number of most significant bits of the rotate up and rotate down signal. Claims 16-18 are therefore believed patentable for reasons similar to claims 10-12, which were indicated to be allowable by the Examiner.

New independent claim 19 recites the subject matter of former claims 1, 2, and 3, which the Examiner indicated was allowable. Claims 20-22 are dependent from claim 19 and similar to claims 3-6, and are believed patentable for at least similar reasons.

New claim 23 is dependent from claim 9 and recites that the combinatorial logic outputs second rotate-up and rotate-down signals which improve a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offset. Claims 23 is patentable over the cited references for at least the same reasons as claims 7 and 9, and for additional reasons similar to those explained above for claim 1.

For the reasons stated hereinabove, Applicants respectfully assert that all claims, as presented in the Amendment, stand ready for allowance and request a Notice of Allowance be timely provided.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited contact the undersigned at the telephone number indicated below.

Respectfully submitted,

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Date

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